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EXAMINER	
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ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/774,374	KAI ET AL.	
	Examiner	Art Unit	
	NELSON D. HERNANDEZ	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Examiner acknowledges the amended claims filed on March 14, 2011. Claims 1, 8 and 12 have been amended.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 8 and 12 have been considered but are moot in view of the new grounds of rejection based on previously cited art (Ohba) previously applied to reject claims 2, 6, 9-14 and 16-19. The Examiner noted that the amendments as presented appear to differentiate from the Waki et al. reference. However, after further consideration of the previously applied prior art, the Examiner noted that the Ohba reference teaches those aspects of the invention presented in the claim as will be discussed in this Office Action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 6-8, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ohba, US Patent 6,714,660 B1.

5. **Regarding claim 1**, **Waki et al.** disclose an integrated circuit (*Fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*), said integrated circuit comprising:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded program needs to be reproduced, the CPU 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2*);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2*), and operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio decoder 306 and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092*); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said

bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086*),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)*), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV*

monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)); and

wherein said second memory is occupied by said second processing unit (*Note that the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner occupies the second memory to read and write image data to be processed (i.e. decompressed. See Col. 14, ¶ 0084-0085)*), such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Note that the limitations as presented do not require that the processor occupies only the second memory. Thus, by teaching that the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) store or access image data to/from the High-Speed Video Memory Unit 307, Memory Unit 310 and Storage Unit 312 as shown in fig. 2, Waki et al. discloses that said second memory (High-Speed Video Memory Unit 307 as interpreted by the Examiner) is occupied by said second processing unit, such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory as claimed*).

Waki et al. does not explicitly disclose that said second memory is occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input*

circuit as claimed) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*), and

wherein said second memory (*Fig. 2: 43*) is occupied only by said second processing unit (*the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner*), when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Ohba discloses that based on a command supplied by the CPU 31, the rendering engine 41 of the image processing chip 33 execute operations that draw the prescribed image data to image memory 43 via memory interface 42, wherein the*

rendering engine 41 executes drawing processing at high speed to image memory 43 (Col. 3, lines 16-28). Also based on an instruction from the CPU 31, the operation of the PCRTC circuit 44 is performed to extract image data from the memory 43 that would later be used by the CPU 31 (Col. 4, line 20 – col. 5, line 62). Thus, considering that the rendering engine 41 and the PCRTC circuit 44 are the processing circuits that access the memory 43 directly, while the CPU only receives data from those processing circuits and not directly from the memory 43, Ohba discloses that said second memory is occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory as claimed).

Therefore, after considering the teaching of Ohba, where the second memory is accessed only by the second processing unit, while the first processing unit only access the image data output from the second processing unit and not directly from the second memory, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. to have the second memory occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory. The motivation to do so would have been to allow high speed processing of the image data that would allow further reception of image data from a camera connected to the integrated circuit to further process the output from the camera to interactively enhance graphic data with features identified from the output of the

camera so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 3, lines 16-28; col. 5, line 63 – col. 6, line 15*).

6. **Regarding claim 2**, **Waki et al.** disclose that said image output circuit generates a video signal for outputting to a display device connectable to said integrated circuit, so as to display an image according to the generated video signal (*The Video/Audio Decoder 306 decompress the video and outputs video signals to a connected TV monitor (Fig. 2: 304) (See col. 14, ¶ 0086)*).

Waki et al. do not explicitly disclose that said image input circuit receives the output image data from a camera device connectable to said integrated circuit.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated

circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, where the second processing unit receives the image data from a camera to further process the image data received from the camera, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the second processing unit in teaching of Waki et al. to further receive image data from a camera connects to the integrated to further process the output from the camera to interactively enhance graphic data with features identified from the output of the camera so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

7. **Regarding claim 6**, Waki et al. do not explicitly disclose that said second processing unit generates computer graphics image data.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), wherein said second processing unit further combine computer graphic with video output from a camera controlled by the CPU 39 (*Fig. 2: 35*) (*See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39).*

Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, which teaches using the second processing unit to create combined image data including computer graphics and video data to modify the second processing unit in Waki et al. to further generate computer graphics image data with the motivation of interactively enhancing the displayed data from the camera with computer graphics so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

8. **Regarding claim 7**, **Waki et al.** disclose further comprising a control unit (*IR Data Send/Receive Unit 311 as shown in fig. 2*) operable to control at least one of said

first processing unit and said second processing unit (*Waki et al. disclose that the IR data send/receive unit 311 receives an IR signal that shows a viewer operation from an operating device (203/204 as shown in fig. 1), and sends data showing the viewer operation to the CPU 309. The viewer operation gives an instruction to the receiving device 202, such as to receive and reproduce a program, to receive and record a program, or to reproduce a program that it has recorded*).

9. **Regarding claim 8**, **Waki et al.** disclose an electric device (*Receiving Device 202 as shown in fig. 1*) comprising:

an integrated circuit (*See fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*); and

a converter (*Video/Audio Decoder 306 as shown in fig. 2, which decompresses the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*),

wherein said integrated circuit comprises:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded program needs to be reproduced, the CPU 309 reads the stored information from the storage*

unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2*), and operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio decoder 306 and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data*

processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086*),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer*

303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*); and

wherein said second memory is occupied by said second processing unit (*Note that the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner occupies the second memory to read and write image data to be processed (i.e. decompressed. See Col. 14, ¶ 0084-0085)*), such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Note that the limitations as presented do not require that the processor occupies only the second memory. Thus, by teaching that the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) store or access image data to/from the High-Speed Video Memory Unit 307, Memory Unit 310 and Storage Unit 312 as shown in fig. 2, Waki et al. discloses that said second memory (High-Speed Video Memory Unit 307 as interpreted by the Examiner) is occupied by said second processing unit, such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory as claimed*).

Waki et al. does not explicitly disclose that said second memory is occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*), and

wherein said second memory (*Fig. 2: 43*) is occupied only by said second processing unit (*the combination of the rendering engine 41 and the PCRTC circuit 44*

as interpreted by the Examiner), when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Ohba discloses that based on a command supplied by the CPU 31, the rendering engine 41 of the image processing chip 33 execute operations that draw the prescribed image data to image memory 43 via memory interface 42, wherein the rendering engine 41 executes drawing processing at high speed to image memory 43 (Col. 3, lines 16-28). Also based on an instruction from the CPU 31, the operation of the PCRTC circuit 44 is performed to extract image data from the memory 43 that would later be used by the CPU 31 (Col. 4, line 20 – col. 5, line 62). Thus, considering that the rendering engine 41 and the PCRTC circuit 44 are the processing circuits that access the memory 43 directly, while the CPU only receives data from those processing circuits and not directly from the memory 43, Ohba discloses that said second memory is occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory as claimed*).

Therefore, after considering the teaching of Ohba, where the second memory is accessed only by the second processing unit, while the first processing unit only access the image data output from the second processing unit and not directly from the second memory, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. to have the second memory occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said

second memory. The motivation to do so would have been to allow high speed processing of the image data that would allow further reception of image data from a camera connected to the electric device to further process the output from the camera to interactively enhance graphic data with features identified from the output of the camera so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 3, lines 16-28; col. 5, line 63 – col. 6, line 15*).

10. **Regarding claim 15**, the Examiner notes that the limitations of claim 15 are written as alternative limitations by reciting "said second processing unit performs at least one of: (i) compressing image data stored in said second memory; (ii) expanding compressed data to image data; (iii) generating image data using a computer graphics operation; and (iv) processing/editing image data, while said first processing unit performs, using said first memory, processing other than the at least of (i), (ii), (iii) and (iv) performed by said second processing unit". **Waki et al.** disclose that said second processing unit performs expanding compressed data to image data (*See col. 14, ¶ 0086*), while said first processing unit performs, using said first memory, processing other than the at least of (i), (ii), (iii) and (iv) performed by said second processing unit (*The first processing unit in Waki et al. performs instructions to control the other processing devices also 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder. See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092*).

11. **Regarding claim 16**, **Waki et al.** disclose that said image output circuit generates a video signal for outputting to a display device connectable to said integrated circuit, so as to display an image according to the generated video signal (*The Video/Audio Decoder 306 decompress the video and outputs video signals to a connected TV monitor (Fig. 2: 304) (See col. 14, ¶ 0086)*).

Waki et al. do not explicitly disclose that said image input circuit receives the output image data from a camera device connectable to said integrated circuit.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the*

second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, where the second processing unit receives image data from a camera to further process the image data received from the camera, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the second processing unit in teaching of Waki et al. to further receive image data from a camera connects to the integrated to further process the output from the camera to interactively enhance graphic data with features identified from the output of the camera so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

12. Claims 3, 4, 17 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ohba, US Patent 6,714,660 B1 and further in view of Kawakami et al., 2002/0012522 A1.

13. **Regarding claim 3**, **Waki et al.** disclose that the second processing unit expands compressed video signals (*col. 14, ¶ 0086*). However, the teaching of Waki et al. in view of Ohba fails to teach that said first processing unit expands compressed audio signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing*

unit) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal Processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video signal processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (*It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (Page 7, ¶ 0144), the reference image data being generated when the compressed video signals are expanded (It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are*

expanded as claimed); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ohba and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught in Kawakami et al. to modify the teaching of Waki et al. and Ohba to have the first processing unit expanding compressed audio signals as an alternative instead of using the second processing unit in Waki et al. while obtaining predictable results (outputting audio signals which have been processed from a different device without changing the main operation of the integrated circuit), and to have the second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (Page 8, ¶ 0144) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

14. **Regarding claim 4**, the combined teaching of Waki et al. in view of Ohba fails to teach that said first processing unit compresses audio signals, wherein said second

processing unit compresses video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video signal Processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (*Page 7, ¶ 0144*), the reference image data being generated when the compressed video signals are expanded (*It is also noted that the MPEG2 compression/decompression uses P-frames*

(Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further teaches that the second processing unit expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ohba and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught in Kawakami et al. to modify the teaching of Waki et al. and Ohba to have the first processing unit compressing audio signals which improve the storage space in memory; to have said second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (*Page 8, ¶ 0144*) to improve the processing units in Waki

et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

16. **Regarding claim 17**, **Waki et al.** disclose that the second processing unit expands compressed video signals to generate video signals (*col. 14, ¶ 0086*) and that the converter convert the audio signals expanded by the second processing unit into analog audio signals (*See col. 14, ¶ 0086. The Examiner understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker*) but do not explicitly disclose that said first processing unit expands compressed audio signals, that said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded, and that said conversion of the audio signals into analog audio signals is performed on audio signals expanded by said first processing unit (being different in that Waki et al. teach that the conversion is made to signals expanded in the second processing unit).

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*), wherein the output of said sound compression

Encoder/Decoder is sent to a converter (*Fig. 4: 65*) to convert the expanded audio signals into analog audio signals to be output to a speaker (*Fig. 4: 205*) (*Page 8, ¶ 0165-0166*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal Processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video signal processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (*It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (Page 7, ¶ 0144), the reference image data being generated when the compressed video signals are expanded (It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed*); and a second

memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ohba and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals that sends the expanded audio signals to a converter to convert the signals into analog signals to be sent to a speaker for reproduction as taught in Kawakami et al. to modify the teaching of Waki et al. to have the first processing unit expanding compressed audio signals to be converter into analog by the converter as an alternative instead of using the second processing unit in Waki et al. and Ohba while obtaining predictable results (outputting audio signals which have been processed from a different device without changing the main operation of the integrated circuit), and to have the second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (Page 8, ¶ 0144) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

23. **Regarding claim 9**, **Waki et al.** disclose that said integrated circuit further comprises a control unit (*IR Data Send/Receive Unit 311 as shown in fig. 2*) operable to control at least one of said first processing unit and said second processing unit (*Waki et al. disclose that the IR data send/receive unit 311 receives an IR signal that shows a viewer operation from an operating device (203/204 as shown in fig. 1), and sends data showing the viewer operation to the CPU 309. The viewer operation gives an instruction to the receiving device 202, such as to receive and reproduce a program, to receive and record a program, or to reproduce a program that it has recorded*).

24. **Regarding claim 10**, **Waki et al.** disclose a display device (*TV monitor 304 as shown in fig. 2*) operable to input the video signals generated by said second processing unit to display an image (*See col. 14, ¶ 0086*); and a playback device (*Speaker 305 as shown in fig. 2*) operable to reproduce sounds according to the analog analogue audio signals converted by said converter (*See col. 14, ¶ 0086. The Examiner understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker*).

25. **Regarding claim 11**, Waki et al. do not explicitly disclose that said second processing unit generates computer graphics image data.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), wherein said second processing unit further combine computer graphic with video output from a camera controlled by the CPU 39 (*Fig. 2: 35*) (*See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input*

circuit as claimed) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, which teaches using the second processing unit to create combined image data including computer graphics and video data to modify the second processing unit to further generate computer graphics image data with the motivation of interactively enhancing the displayed data from the camera with computer graphics so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

17. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ohba, US Patent 6,714,660 B1 and further in view of Applicants Admitted Prior Art (thereinafter referred as AAPA).

18. **Regarding claim 5**, the combined teaching of Waki et al. in view of Ohba fails to teach that said first processing unit performs at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream.

However, **AAPA** teaches an integrated circuit comprising: a bus (*Fig. 2: 2*); a first memory connected to said bus (*Fig. 2: 3*); a first processing unit (Fig. 2: 6) operable to access said first memory via said bus (*See fig. 2*) and operable to perform at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream (*Page 2, ¶ 0012-0015*); a second processing unit (*Fig. 2: 4*) operable to access said first memory via said bus (*See fig. 2*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*Video processing unit 4 perform image processing which requires more capacity that the audio processed by audio processor 5*); and a second memory (*buffer 7 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus (*Note that the buffer 7 is operable to be directly accessed by the second processing unit as shown in fig. 2*).

Therefore, taking the combined teaching of Waki et al. in view of Ohba and further in view of AAPA as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of having a

multiplex/de-multiplex circuit for de-multiplexing audio signals and video signals from a bit stream or multiplexing audio signals and video signals into a bit stream to have the first processing unit performing at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream as an alternative to the second processing unit as it is done in Waki et al. with the motivation of providing a multiprocessor configuration in which different processors perform specific operation as taught in AAPA.

19. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohba, US Patent 6,714,660 B1 in view of Waki et al., EP 1056290 A2.

20. **Regarding claim 12**, **Ohba** discloses an electric device comprising:

a camera (*Fig. 2: 35*);

a microphone (*Fig. 2: 38*);

an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*); and

a converter (*Ohba discloses the use of an audio processing chip (Fig. 2: 37) that received audio data input by the microphone 38 to transmit the audio data through the internet to another image processing device (Col. 3, lines 40-48). This teaches the use of a converter as claimed*),

wherein said integrated circuit comprises:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note that memory 32 is connected to said bus 34 as shown in fig. 2*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*), and operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), in a larger amount than said first processing unit (*The rendering engine 41 and PCRTC 44 perform drawing processing at high speed to an image memory 43, while the PCRTC control in real time the position, size and resolution of the image data input from the camera 35 to send the modified video signal to a CRT monitor 36 (Col. 3, lines 16-39) while the first processing unit 31 controls the operation of the processing unit 33 (which includes the second processing unit), generate processing commands to said second processing unit (Col. 3, lines 10-15) and perform feature extraction on the received video to be latter combined to the computer graphics in the rendering engine and the PCRTC (Col. 4, lines 20-28, lines 46-53; col. 5, lines 3-18). It is noted that in combination, the rendering engine 41 and the PCRTC circuit 44 (which is being interpreted as the second processing unit as claimed), perform larger amount of processing than said first processing unit*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit

accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*), and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component (*Camera 35 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*), and

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine*

41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)).

wherein said second memory (*Fig. 2: 43*) is occupied only by said second processing unit (*the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner*), when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Ohba discloses that based on a command supplied by the CPU 31, the rendering engine 41 of the image processing chip 33 execute operations that draw the prescribed image data to image memory 43 via memory interface 42, wherein the rendering engine 41 executes drawing processing at high speed to image memory 43 (Col. 3, lines 16-28). Also based on an instruction from the CPU 31, the operation of the PCRTC circuit 44 is performed to extract image data from the memory 43 that would later be used by the CPU 31 (Col. 4, line 20 – col. 5, line 62). Thus, considering that the rendering engine 41 and the PCRTC circuit 44 are the processing circuits that access the memory 43 directly, while the CPU only receives data from those processing circuits and not directly from the memory 43, Ohba discloses that said second memory is occupied only by said second processing unit, when said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory as claimed*).

The teaching of Ohba is different from claim 12 in that claim 12 further requires that the second processing unit is operable to access said first memory via said bus.

However, **Waki et al.** disclose an integrated circuit (*Fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*), said integrated circuit comprising:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded program needs to be reproduced, the CPU 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2*);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2*), and

operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio decoder 306 and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092*); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086*),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit*

includes an image input circuit as claimed) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)*), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*); and

wherein said second memory is occupied by said second processing unit (*Note that the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner occupies the second memory to read and write image data to be processed (i.e. decompressed. See Col. 14, ¶ 0084-0085)*), such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory (*Note that the limitations as presented do not require that the processor occupies only the second memory. Thus, by teaching that the second processing unit (the combination of the Video/Audio Decoder 306 and*

Demultiplexer 303 as interpreted by the Examiner) store or access image data to/from the High-Speed Video Memory Unit 307, Memory Unit 310 and Storage Unit 312 as shown in fig. 2, Waki et al. discloses that said second memory (High-Speed Video Memory Unit 307 as interpreted by the Examiner) is occupied by said second processing unit, such that said second processing unit stores image data related to at least one of the output image data and the video signal in said second memory since).

Therefore, taking the combined teaching of Ohba in view of Waki et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of having a second processing unit which is connected to a bus to access a further memory through the bus as taught in Waki et al. to modify the teaching of Ohba to allow the second processing unit to access the first memory via said bus with the motivation of allowing recording data processed by the second processing unit on a further dedicated high speed memory as suggested by Waki et al. (*Col. 15, ¶ 0091, see also col. 14, ¶ 0086*).

21. **Regarding claim 18**, **Ohba** discloses that said image input circuit receives the output image data from said camera (*Ohba discloses that the PCRTC 44 receives the image data from the camera 35*), which is connectable to said integrated circuit (*Note that the camera is connectable to said integrated circuit as shown in figs. 2, 6 and 12*) (*See col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*), and wherein said image output circuit generates a video signal for outputting to a display device (*CRT monitor as shown in fig. 2*) connectable to said integrated circuit block (*Note that*

the monitor is connected to said integrated circuit as shown in figs. 2, 6 and 12), so as to display an image according to the generated video signal (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (See col. 3, lines 29-39)*).

26. Claims 19, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ohba, US Patent 6,714,660 B1 and further in view of Kawakami et al., 2002/0012522 A1.

27. **Regarding claim 19**, Ohba discloses that said converter (*Fig. 2: 37*) is operable to input analog audio signals from said microphone to convert the analog audio signals into digital audio signals (*Ohba discloses that the audio processing receives audio data input by the microphone 38 to transmit the audio data through the internet to another image processing device (Col. 3, lines 40-48). This teaches that the converter converts the analog audio signals into digital audio signals since in order to transmit the audio signals, said signals need to be converted to digital format to be transmitted through the internet*), and operable to output the digital audio signals to said first processing unit (*The main CPU 31 (first processing unit as claimed) controls the audio processing chip and causes audio data from the microphone to be transmitted from communication unit through internet to a server. See col. 7, lines 4-7*) and Waki et al. teaches that the second processing unit expands compressed video signals to generate video signals (*col. 14, ¶ 0086*) and that the converter convert the audio signals expanded by the second processing unit into analog audio signals (*See col. 14, ¶ 0086. The Examiner*

understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker) which would be advantageous to include in the Ohba teaching with the motivation of allowing reception of compressed images that would reduce the transmission time of said image signals to the integrated circuit.

The combined teaching of Ohba in view of Waki et al. fails to teach that said first processing unit compresses audio signals, that said second processing unit inputs video signals from said camera to compress the video signals, that said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal processing requires calculation in a larger*

amount than the sound compression Encoder/Decoder), wherein the MPEG2 video signal Processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (*Page 7, ¶ 0144*), the reference image data being generated when the compressed video signals are expanded (*It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further teaches that the second processing unit expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed*); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Ohba in view of Waki et al. and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught in Kawakami et al. to modify the teaching of Ohba and Waki et al. to have the first processing unit

compressing audio signals which improve the storage space in memory; also to have said second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (*Page 8, ¶ 0144*) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

28. **Regarding claim 13**, **Ohba** discloses that the second processing unit generates computer graphics image data (*The second processing unit combines computer graphic with video output from a camera controlled by the CPU 39 (Fig. 2: 35) (See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15). This teaches that the second processing unit generates computer graphics image data as claimed*).

29. **Regarding claim 14**, **Ohba** discloses that said integrated circuit further comprises a control unit (*Input Unit 30 as shown in fig. 2*) operable to control at least one of said first processing unit and said second processing unit (*The user operates the input unit 30 and the CPU 31 operates in accordance to the inputs made by the user. See Col. 6, line 16 – col. 7, line 3*).

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NELSON D. HERNANDEZ whose telephone number is (571)272-7311. The examiner can normally be reached on 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/NELSON D HERNANDEZ/
Primary Examiner, Art Unit 2622
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